MAINTENANCE MANUAL
AUDIO/LOGIC BOARD
19D903963G1

TABLE OF CONTENTS

DESCRIPTION

Audio/Logic Board 19D903963G1 is used in MDR and MDX mobile radios. This board contains microprocessor circuitry used to control the radio's RF circuits, handset circuits (MDR radios only), and display board circuits (MDX radios only). The board also has the audio signal processing circuitry and support circuitry for the Aegis and Data Radio options.

The Audio/Logic Board mounts on the bottom of the frame assembly. Connectors on the board interconnect the RF Board and the Audio Amplifier Board (or Radio Interface Board for the MDX remote mount applications). An option connector is used for interface of the Aegis and Data Radio options.

The Audio/Logic Board contains the following major components:

- 8-bit microcontroller
- 128K x 8-bit operational software memory (flash EEPROM)
- 8K x 8-bit personality memory (EEPROM)
- 8K x 8-bit temporary storage and data memory (RAM)
- 4800/9600 baud modem
- serial number memory (ROM)
- audio signal processor, busy tone notch filter and high-pass filter
- DTMF tone generator
- public address circuitry
- duplex sidetone cancellation circuitry
- Aegis interface and external Data Radio interface circuitry
- 5-Volt and 8-Volt regulators

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CIRCUIT ANALYSIS

MICROCONTROLLER U701

Microcontroller U701 controls the operation of the radio. This integrated circuit is an Intel 83C51 8-bit microcontroller with extensive I/O (Input/Output) interface and controlling capabilities. The microcontroller performs the following radio functions:

- EDACS trunking functions
- GE-MARC trunking functions
- conventional mobile radio functions
- synthesizer loading and lock monitoring
- squelch control
- transmit control
- high-speed data decoding and encoding through the modem
- low-speed data and Channel Guard decoding and encoding
- alert tone generation
- DTMF tone generation through the DTMF generator
- audio path enable/mute control
- transmit and receive level adjust
- handset serial communication (MDR radios)
- display board serial communication (MDX radios)
- GE-MARC standard/alternate busy tone notch selection
- external horn relay control and public address relay control
- operational radio code flash programming
- personality programming
- clock oscillator shift control

Operating Program

The radio's operating program is stored in 128K x 8-bit flash EEPROM U703. Microcontroller U701 executes this program during normal radio operations. During flash programming operations U701 runs a masked program stored in itself to transfer the new data arriving from flash programming equipment into U703. See the section entitled **"FLASH EEPROM U703"** for additional details on U703.

Clock Circuitry

An 11.0592 MHz clock for U701 is generated from a clock oscillator circuit in modem U702 using 11.0592 MHz crystal Y701. This clock signal is applied to U701 pin 52 and it sets the ALE (Address Latch Enable) output pulse frequency on U701 pin 55 to 1.8432 MHz (0.54 microsecond period). The PSEN (Program Store ENable) output at U701 pin 54 also runs continuously at 1.8432 MHz except when U701 accesses external memory.

Handset/Display Interfacing

Interfacing between microcontroller U701 and the MDR handset is by a 300 baud serial data stream on DISPLAY_SERIAL (J701 pin 6) and KEYPAD_SERIAL (J701 pin 1). The microcontroller updates the handset's display by sending data over DISPLAY_SERIAL. Keypad data from the handset is sent to U701 by the KEYPAD_SERIAL line. Both of these serial data lines remain at a high state when data is not being transferred.

Interfacing between microcontroller U701 and the Display Board in an MDX radio is by 9600 baud serial data streams using the DISPLAY_SERIAL (J701 pin 6), KEYPAD_SERIAL (J701 pin 1) and SERIAL_RQST (J701 pin 7) lines. The microcontroller transmits display data to the Display Board at 9600 baud rates via DISPLAY_SERIAL. When a key is pressed on the Display Board's keypad, the Display Board first pulls the SERIAL_RQST line low to signal microcontroller U701 that a key has been pressed. Next, U701 signals the Display Board via the DISPLAY_SERIAL line that it is ready to accept the keypad data. The Display Board then sends the keypad data to U701 at 9600 baud via KEYPAD_SERIAL. When data is not being transferred, these data lines remain high.

The DISPLAY_SERIAL and KEYPAD_SERIAL lines are also used for flash and PC personality programming.

RF Board Interfacing

Microcontroller U701 loads the synthesizer circuits on the RF Board using the S_DATA (J702 pin 10), S_CLK (J702 pin 11) and S_ENABLE (J702 pin 9) lines. U701 monitors synthesizer lock status via the LOCK_DET line (J702 pin 12) from the RF Board. This line is high when the synthesizer is locked.

Bandswitch control for the transmit talk-around frequencies is accomplished with the BANDSWITCH line (J702 pin 5) from U701. U701 switches BANDSWITCH low when the radio is operating on a talk-around channel.

A delayed PTT line, DPTT (J702 pin 7), goes low after all transmit functions have been enabled. It remains low for the duration of the transmit key. This line enables the transmit circuitry on the RF Board.

Audio Signal Processor Control

Microcontroller U701 controls ASP (Audio Signal Processor) U804 using the ASP DATA (U701 pin 10), ASP STB (U701 pin 11), and ASP EN (U701 pin 12) lines. These logic lines from U701 load the registers inside the ASP that control its internal audio paths and level control circuitry. ASP DATA is the data line, ASP STB is the strobe (clock) line and ASP EN is an enable line. See the section entitled **AUDIO SIGNAL PROCESSOR U804** for detailed information on the audio signal paths and interfacing of the ASP.

Address Demultiplexing

The upper address byte is applied directly to the memory chips via U701's eight outputs, A8 - A15. The lower address byte is multiplexed with data on the 8-bit wide address/data bus. This bus transfers both the lower address byte and the 8-bit bi-directional data. Before the microcontroller can read or write data, the lower address byte must first be externally latched and applied to the memory chips. Modem U702 contains an 8-bit latch which provides this demultiplexing function for U701.

The ALE output line from U701 is applied to U702 pin 12. The lower address byte (A0 - A7) is latched when the ALE line transitions from high to low. The latched byte is applied to U703, U707 and U802 via the eight outputs (A0 - A7) from U702.

Address Decoding And Processor Control Outputs

This memory-mapped system uses a decoder in modem U702 to provide address decoding (chip selection) for the modem, the RAM, EEPROM and optional Aegis Board. Four (4) active low outputs from U702 (Q0 - Q3) are applied to the RAM (Q0 at pin 30), EEPROM (Q1 at pin 29), the Aegis Board (Q2 on pin 28) and the modem chip (Q3 on pin 27).

Microcontroller U701 generates the active low write (WR) and read (RD) pulses for the external memory-mapped devices at U701 pins 37 and 38 respectively. U701 reads the external EEPROMs when the program store enable (PSEN) line from U701 pin 54 is low.

The microcontroller addresses the upper 64K bank of memory in 128K flash EEPROM U703 using the output on U701 pin 21. This line is connected to U703's A16 address input.

FLASH EEPROM U703

The radio's operating program is stored in 128K x 8-bit flash EEPROM U703. Microcontroller U701 executes this program during normal radio operations.

EEPROM U703 can be "flashed" to upgrade the operating program. This process allows easy reprogramming of the radio's firmware for upgrades and when additional features are added. During flash programming operations, microcontroller U701 runs a simple masked program stored in itself to transfer the new data arriving from the flash programming equipment into U703. This provides easy reprogramming without the need to disassemble the radio. Flash programming equipment is connected to J701 and it uses the same interface circuitry (DISPLAY_SERIAL and KEYPAD_SERIAL) that is used to program the personality into EEPROM U802.

The microcontroller is placed in the flash program execution mode by the presence of 12 Vdc on PTT/FLASH_VPP/EXT_SPKR_MUTE (J701 pin 2). The flash program is then executed by sending a proprietary protocol on the DISPLAY_SERIAL and KEYPAD_SERIAL data lines. With 12 Vdc applied to J701 pin 2, transistors Q801 and Q802 turn on. The collector of Q802 applies 12 Vdc to the VPP input of U703 and voltage divider R726 and R727. The voltage divider pulls the EA/VPP input at U701 pin 56 high (5 Volts) to enable flash programming mode.

The microcontroller uses the A15 ENBL line (U701 pin 36) during flash programming to isolate writes to U703. In normal radio operation, this line is always high to enable the A15 address line from the U701 pin 64 to arrive at the U703 pin 11 via Q701. The address bank select line, U701 pin 21, is used to switch the flash memory bank from the lower 64K bank (when U701 pin 21 is low) to the higher 64K bank (when U701 pin 21 is high) of the 128K x 8-bit total flash memory. R780 and C780 provide a delay of this bank select line to synchronize to the other address lines.

NOTE

The flash memory requires a precise voltage of 11.5 to 12.5 Vdc for proper programming. This voltage is applied at the radio's PC and Flash programming port. Damage to the flash memory and other devices will result if the flash voltage on J701 pin 2 exceeds 12.5 Vdc.

PERSONALITY EEPROM U802

All personality data is stored in 8192 x 8-bit EEPROM U802. This data, programmed with the PC programming equipment, includes systems, groups, special call information, frequencies, tones, option information, mic deviation levels, data deviation levels, squelch levels, and the current receiver volume level. There is also a unique serial number stored in the EEPROM that must match the serial number stored in serial number ROM U706. EEPROM U802 is programmed through the same PC programming interface that programs flash EEPROM U703.

The DISPLAY_SERIAL and KEYPAD_SERIAL data lines are used for the PC programming interface. PC programming is invoked in normal radio mode by a proprietary protocol on the DISPLAY_SERIAL and KEYPAD_SERIAL data lines.

NOTE

If U802 or U706 replacement is necessary, contact Ericsson Technical Assistance Center to obtain programming information.

RAM U707

Integrated circuit U707 is an 8192 x 8-bit high-speed static RAM that provides temporary data storage for microcontroller U701. When the board is used in an MDX remote mounted installation, U707 also provides buffering for data to and from the RDI (Radio Data Interface).

Thirteen (13) address lines are applied to the RAM. The lower eight address lines (A0 - A7) are applied to it from the 8-bit demultiplexer address latch inside modem U702. The higher five address lines (A8 -A13) are applied directly from U701.

RAM chip selection is accomplished with the active-low chip select pulse (U707 pin 20) from the modem. Read/write control is achieved with the output enable input (OE at U707 pin 22) and the active-low write enable input (WR at U707 pin 27) from U701.

MODEM U702

Modem U702 performs several important functions for the Audio/Logic Board. These functions include:

- high-speed data parallel-to-serial and serial-to-parallel conversions
- address demultiplexing for the microcontroller's lower address byte (A0 - A7) from the address/data bus
- address decoding (chip selection) for itself and the other memory-mapped integrated circuits
- reset logic for the microcontroller and the ASP
- 11.0592 MHz clock generation for itself, the microcontroller and the ASP

High-Speed Data Conversions

Modem U702 converts high-speed EDACS data between parallel and serial formats. High-speed rates are 9600 baud for 800 MHz radios and 4800 baud for 900 MHz radios.

When the radio is receiving high-speed data, U702 converts this serial data to parallel data that can be handled by the microcontroller. Limited high-speed data from ASP (Audio Signal Processor) U804 feeds U702 pin 23.

When the radio is transmitting high-speed data, the modem converts the parallel data from the microcontroller to serial high-speed data that can modulate the transmitter. This data is routed to the transmit audio portion of the ASP via U702 pin 26.

An interrupt output from U702 pin 32 signals U701 pin 34 that the modem is ready for the next transmit or receive byte.

Address Demultiplexing

The microcontroller has a multiplexed 8-bit wide address/data bus that transfers both the lower eight address lines and the 8-bit bi-directional data. Before the microcontroller can read or write data, the lower address byte must first be externally latched and applied to the memory chips. Modem U702 contains an 8-bit latch which provides this demultiplexing function.

The microcontroller's ALE output line is applied to U702 pin 12. The lower address byte (A0 - A7) is latched when the ALE line transitions from high to low. The latched byte is applied to U703, U707 and U802 via the eight outputs (A0 - A7) from U702.

Address Decoding

Another function of the modem is to provide address decoding (chip selection) for itself, the RAM, EEPROM and optional Aegis Board. Four (4) active low outputs from U702 (Q0 - Q3) are applied to the RAM (Q0 on pin 30), EEPROM (Q1 on pin 29), the Aegis Board (Q2 on pin 28) and the modem chip itself (Q3 on pin 27).

Reset Logic

A reset pulse from U702 pin 43 is applied to the microcontroller and the ASP at the following states:

- at power-up
- if the watchdog timer circuit in U702 times out
- if the +5 Vdc regulated supply from U801 falls out of regulation

This active-high reset pulse is inverted by NAND gate U708 and applied to the active-low reset inputs of the microcontroller (U701 pin 30) and the ASP (U804 pin 9).

A watchdog timer inside the modem must be serviced by the microcontroller at least every two (2) seconds or a 50 microsecond wide reset pulse will be sent to the microcontroller and the ASP. This will occur if a hardware or software failure develops.

The modem receives a reset signal generated by +5 Vdc regulator U801 when the radio is powered-up and if the +5 Vdc supply falls out of regulation. Transistor Q804 inverts the reset line from U801. This reset input to the modem on U702 pin 33 (RESIN) is low during normal radio operation. At power-up, U801 and Q804 pull U702 pin 33 low after the +5 Vdc supply becomes stable. U702 then brings its reset output on pin 43 low and the microcontroller and the ASP begin to operate. If the +5 Vdc supply falls out of regulation (less than 4.75 Vdc), U801 will pull U702 pin 33 high (via Q804) and U702 will then reset the microcontroller and the ASP by pulling its reset output (U702 pin 43) high.

Clock Circuitry

A clock oscillator circuit in U702 generates an 11.0592 MHz clock for the microcontroller and the ASP. Crystal Y701 is the frequency reference component. The buffered clock signal at U702 pin 15 is sent to the microcontroller and the ASP.

This 11.0592 MHz clock frequency can be slightly shifted if a clock harmonic or interfering signal ("birdie") falls on the current receive frequency. This oscillator shift function is enabled with the PC Programmer on a per channel basis. When the shift is enabled on the current receive frequency, microcontroller turns Q702 on via an output from the ASP (U804 pin 15). With Q702 on, additional capacitive loading is applied to the crystal via C735.

SERIAL NUMBER ROM U706

The serial number ROM (Read Only Memory) U706 contains a unique 48-bit number which is read by the microcontroller at power-up. A single pin on the device provides serial communication with the micro as well as +5 Vdc power through pull-up resistor R728.

For proper radio operation, the unique serial number must match the personality information in EEPROM U802. Replacing either device may disable operation on all programmed EDACS systems. Conventional and GE-MARC systems will continue to function normally. To restore EDACS operations, the radio must be reprogrammed based upon the serial number.

NOTE

If replacement of U706 serial number ROM or U802 personality EEPROM is necessary, contact Ericsson Technical Assistance Center to obtain programming information.

AUDIO SIGNAL PROCESSOR U804

Integrated circuit U804 is the ASP (Audio Signal Processor) that handles most of the audio functions for the radio. The following outline describes basic signal paths for the various operating modes.

Receive Audio Paths

EDACS & Conventional RX Audio Modes

The VOL/SQ_HI detector audio from the receiver (J702 pin 4) is applied to the inverting (-) input of the op amp buffer stage in the ASP. This input is on U804 pin 44 which is biased to "virtual ground". R609 and R610 set the gain of the op amp. Typical signal level at J702 pin 4 is 150 mV rms.

In the ASP, the buffered detector audio is 300 to 3000 Hz bandpass filtered, applied to a multiplex switch (ISA/ISB), and then passed through de-emphasis stages. The de-emphasized audio then passes through a digital volume control (RA0 - RA5) and an audio switch (RXO) before it is applied to the ASP's receive audio output terminal at U804 pin 27. The receive audio path for EDACS and conventional modes never loops out and back into the ASP.

Receive audio from U804 pin 27 feeds amplifier U301.1 through FET switch Q640. Transistor Q640 passes the audio to U301.1 only when the SW0 output of the ASP (U804 pin 18) is high. Q640 provides full muting of the RX_AUDIO signal.

High-Speed Data Limiter

In the ASP, buffered and unfiltered audio from the input buffer stage passes through an audio switch (TDS) to pin 45. Busy tone decode switch Q603 is normally off (SW5 is high) so data pass through R612 to the non-inverting (+) input (U804 pin 32) of a comparator in the ASP. This comparator forms the high-speed data limiter. The average dc level of the serial data signal is applied to the comparator's inverting (-) input as a dc reference for the comparator. R611 and C605 filter the signal component to provide the dc reference. R621 adds hysteresis to this stage.

The output of the limiter stage (U804 pin 21) is inverted by Q602 and the serial data is applied to the modem for serial-to-parallel conversion. It is also connected to microcontroller U701 pin 7; this pin is normally at a high impedance but it is switched low during transmit to clamp limited noise out of the modem's receive data input.

Transistor Q601 on the VOL/SQ HI line allows the high-speed and low-speed data limiters to settle quickly after the receiver locks on to a new frequency. Since the charge across C601 can change significantly during a frequency change, the positive end of C601 must be quickly brought back to 2.5 Vdc before the limiters can function properly. Q601 is turned on for 5 - 10 milliseconds after the synthesizer locks via the SW1 output from the ASP (U804 pin 17). Since the VOL/SQ_HI output impedance of the RF Board is relatively low (less than 500 ohms), this action charges C601 to 2.5 Vdc considerably fast.

Low-Speed Tone/Data Decoding

In the ASP, buffered detector audio from the input buffer stage passes through an audio switch (TX) and feeds a low-pass filter that removes all voice signals. The filter's output is any low-frequency CG (Channel Guard) tones or low-speed data signals present in the received signal. Cutoff for this low-pass filter is switched to 105 Hz when the programmed CG decode tone is equal to or less than 105 Hz. The filter is switched to a cutoff of 210 Hz if the programmed CG decode tone is greater than 105 Hz or if the radio is in data decode mode.

The output of the low-pass filter passes through an audio switch (CGE) and then out of the ASP via U804 pin 37. The tones/data feed U802 pin 35 which is the non-inverting (+) input to a comparator that forms the low-speed data limiter. The average dc level of the tones/data signal is applied to the inverting (+) input of the comparator as a dc reference. R618 and C610 filter the signal to provide the dc reference. The output of the limiter on U804 pin 22 is applied to microcontroller U701 pin 8 for decoding.

GE-MARC Mode RX Audio

Detector audio enters the ASP at U804 pin 44. In the ASP, this audio is buffered, 300 - 3000 Hz bandpass filtered, and then passed through a switch (TDS) to the output on U804 pin 45. The filtered receive audio is then applied to U602 which is a digital switch capacitance notch filter. Notch frequency is determined by ceramic resonators Y601 or Y602. These resonators allow detection of the standard 3052 Hz busy tone or the alternate 2918 Hz busy tone. The output from microcontroller U701 pin 22 selects the proper resonator by turning on either Q606 or Q607.

The output of the notch filter is U602 pin 9 (VOUT). During reception, Q605 is turned on by a low from U701 pin 18. This action applies the notched audio to the ASP at U804 pin 28. In the ASP, the multiplex audio switch (ISA/ISB) routes the notched audio to the digital volume control. The output of the volume control is routed through another switch (RXO) and leaves the ASP on U804 pin 27 to be amplified by U301.1 and the Audio Amplifier Board.

GE-MARC Tone Decoding

Bandpass filtered detector audio on U804 pin 45 is applied to notch filter U602, bandpass filter U601.2 & U601.1, and the high-speed limiter.

For signaling tone decode, busy tone decode switch Q603 is off since the SW5 output from the ASP (U804 pin 13) is high. Wide-band audio passes from U804 pin 45 through R612 to the non-inverting input (U804 pin 32) of the comparator in the ASP. This comparator forms the high-speed data limiter. The average dc level of the signal is applied to the comparator's inverting input (U804 pin 31) as a dc reference for the comparator. R611 and C605 filter the signal component to provide the dc reference. The output of the limiter (U804 pin 21) is sent to microcontroller U701 pin 7 for tone decoding.

During a busy tone decode (Q603 is on), bandpass filtered audio at the busy tone frequency feeds the high-speed data limiter through U601.2, U601.1 and Q603. Since the output impedance of U601.1 is very low and Q603 is on, wide-band audio from U804 pin 45 is greatly attenuated across R612. The 3 kHz low-pass filtered audio from U804 pin 45 provides some of the high-frequency roll off. U601.2 provides a notch at 2.3 kHz plus a high-pass response to reject voice frequencies. U601.1 is a bandpass filter centered at 3 kHz. From this point, the busy tones are decoded similarly to signaling tone decodes.

Receive Noise Squelch

The squelch circuit monitors the detector's high-frequency noise level to determine if a carrier is quieting the receiver. A D/A (Digital-to-Analog) converter in the ASP sets the squelch threshold level. This level is normally 8 dB SINAD. When receiver noise falls below the threshold level, the ASP CAS (Carrier Activity Sensor) output at U804 pin 23 switches low. The ASP CAS signal feeds the input on microcontroller U701 pin 43.

Buffered and unfiltered detector audio leaves U804 pin 43 and feeds pin 50 which is the input to the squelch high-pass filter (7.5 kHz for 800 MHz radios or 4.5 kHz for 900 MHz radios). In the ASP, the high-pass filtered audio is rectified and sent out on U804 pin 52. The rectified noise is filtered by C612 (and C611 if Q604.1 is on) to provide an average dc level proportional to receiver noise level. This dc level is applied to a non-inverting dc buffer amplifier at U804 pin 55. The output of the amp is on U804 pin 53. The gain of the dc amp is set by R620, R622, R623 and thermistor RT601. The thermistor increases in resistance at colder temperatures therefore causing an increase in the dc amp's gain. This compensates for a decrease in receiver noise level from the RF Board at colder temperatures.

The buffered dc level that is tracking receiver noise level is sent to a comparator's inverting (-) input at U804 pin 49. This comparator's non-inverting (+) input is set to a voltage generated by the D/A converter in the ASP. The comparator's output switches high when the dc level tracking receiver noise falls below the comparator's reference level. This output is inverted and it appears at U804 pin 23. This ASP CAS output is normally high and switches low when a carrier is detected.

To tighten the squelch, the D/A reference voltage is lowered. Hysteresis for the squelch is done with software. When the ASP CAS output switches to indicate a signal is detected, the D/A reference value is increased slightly to loosen the squelch. This action eliminates "bubbling" or chattering noises in the speaker. "Bubbling" is normally caused by changes in the dc level around the reference point.

Transistor Q604.1 is normally turned on via the SW2 output at U804 pin 16 (SW2 = high). This action places C611 into the dc level averaging circuit. C611 provides slow squelch (60 ms) operation to prevent audio chopping with rapid squelch closings in weak signal areas. When Q604.1 is turned off, a 5 ms fast squelch is provided by only C610.

Receive Alert Tones

The programmable alert tones are generated in the ASP using a 66.6 kHz clock divided by a 6-bit divider and then divided by two. Therefore, the lowest alert tone frequency that can be generated is 66.6 kHz divided by 64 then divided by 2 = 520 Hz.

The output of the alert tone divider is on U804 pin 76. This output connects back to U804 at pin 30 to feed the audio multiplex switch (ISA/ISB) in the receive audio path. The tones then pass through de-emphasis stages. The de-emphasized audio passes through the digital volume control, through an audio switch (RXO), and then to U804 pin 27 to feed amplifier U301.1 and the Audio Amplifier Board.

Transmit Audio Paths

Transmit Mic Audio

The microphone receives a dc bias through R315. Mic audio is coupled into U804 pin 74 via plug P7 on J910, C303 and R318. In the ASP, mic audio passes through an audio switch (MIS) to the microphone amplifier. A second switch in the mic amp circuit (MGS) sets the gain of the mic amp. This switch is normally closed for low gain. The audio from the mic amp is then pre-emphasized and 300 Hz high-pass filtered. The mic audio then leaves the ASP on U804 pin 70.

Pre-emphasized mic audio is coupled into U804 pin 57 by C304. The audio is passed through muting switch (AEN) and then it feeds the limiter circuit. This limiter's threshold can be stepped up by the microcontroller so peak deviation of the mic audio can be increased when no Channel Guard is present.

Limited mic audio then passes through the summing amp in the ASP which sums the mic audio, tones and data. The output of the summing amp feeds a switch (PBY) that switches the mic audio to the 3 kHz post limiter filter (for limited mic audio) or directly to the transmit deviation level control circuit in the ASP for data transmissions. The output of the digital deviation control the passes to the output on U804 pin 60.

The TX audio (TX_AU) output from the ASP feeds U301.3 and U301.4 which provides two functions. U301.3 provides low-frequency equalization (bass boost) for the synthesizer below 20 Hz. This equalization compensates for low-frequency roll-off normally experienced when modulating the VCO in RF synthesizers. U301.4 is a second-order (12 dB/octave) low-pass filter stage used to attenuate any out-of-band noise from the ASP above approximately 10 kHz. The output from U301.4 (TX MOD) is dc coupled to the RF Board to feed the synthesizer by J702 pin 8.

The bass boost function of U301.3 can be enabled or disabled by jumper J1 and shorting plug P1. The bass boost function is disabled (bypassed) when P1 is placed across J1 pins 1 and 2. Base boost is enabled when P1 is placed across J1 pins 2 and 3.

High-Speed Data Encoding

When the radio is transmitting high-speed data, the serial data from the modem is applied to U804 pin 80. Inside the ASP, this data passes through a bessel filter and then the output of the filter is sent to the TX summing amplifier. The output of the summing amplifier feeds an audio switch (PBY) to allow 3 kHz post limiter filter bypassing during data transmissions. The data then passes through the digital deviation control and then through an audio switch (TXO) to feed U301.3 and U301.4 and the synthesizer.

During high-speed data transmissions, the modem input from the receive data limiter requires muting to prevent the modem from being disturbed by excessive receiver noise. Microcontroller U701 pin 7 switches low during transmit to clamp the line to ground.

CG Tones And Low-Speed Data Encoding

Microcontroller U701 generates the low-frequency Channel Guard tones and low-speed data using its WB1 and WB2 walsh bit outputs. These two bits are also used to generate GE-MARC signaling tones as described in the following section entitled **"GE-MARC Signaling Tone Encoding".**

The 2-bit low-frequency walsh bits are summed into the ASP at U804 pin 38. These stepped tones or data pass through an audio switch (TX) in the ASP and then the 105/210 Hz low-pass filter. Cutoff for this filter is switched to 105 Hz when the programmed CG encode tone is equal to or less than 105 Hz. The filter is switch to a cutoff of 210 Hz if the programmed CG encode tone is greater than 105 Hz or if the radio is in data encode mode.

The filtered tones/data pass through a gate (CGE) and then out of the ASP at U804 pin 37, through R309 via the TX_CG line, and back into the ASP on U804 pin 58 (CGIN). GE-MARC busy tones are also fed into this pin through C310.

In the ASP, the filtered tones/data pass from U804 pin 58 (CGIN) through an audio switch (BEN) to feed the transmit summing amplifier. The output of the summing amp feeds another switch (PBY) that switches the 3 kHz post limiter filter in-line. The output of the post limiter passes through the digital deviation control, through another switch (TXO), and then out of the ASP to U301.3 and U301.4. See the section entitled **"Transmit Mic Audio"** for details on U301.3 and U301.4.

GE-MARC Signaling Tone Encoding

Microcontroller U701 generates the GE-MARC signaling tones using its WB1 and WB2 walsh bit outputs. These two bits are also used to generate Channel Guard tones and low-speed data as described in the previous section entitled **"CG Tones And Low-Speed Data Encoding".**

The 2-bit generated GE-MARC tones feed U804 pin 59. In the ASP, the tones pass through an audio switch (DEN) and they are then sent to the summing amplifier in the TX audio path. The tones are next routed to the 3 kHz post limiter filter through another audio switch (PBY) and then they are filtered, sent through the digital deviation control, via an audio switch (TXO) and then out of the ASP on U804 pin 60.

GE-MARC Busy Tone Encoding

Microcontroller U701 pin 27 generates either the standard 3052 Hz or the alternate 2918 Hz busy tone. This square wave signal is summed into the TX audio path at the same point as the low-frequency CG tones/data at U804 pin 58 (CGIN). C752, R753 and R316 determine the 1 kHz deviation level. C310 couples the tone into U804 pin 58. The tones then follow the same path in the ASP as the CG tones/data.

DTMF Tone Encoding

Encoder U803 generates DTMF tones during conventional mode DTMF dialing and trunked mode DTMF overdial operations. U803 pin 5 feeds U804 pin 73. In the ASP, an audio gate (MIS) passes the DTMF tones to the mic amp while muting the mic audio. A second switch in the mic amp circuit (MGS) determines the mic amp gain; it is set for high gain during DTMF transmissions. The amplified DTMF tones are then pre-emphasized and follow the same path as the mic audio.

To provide DTMF sidetone operation, the DTMF tones are also fed to the receive audio path via U804 pin 29 . The sidetone audio is selected by the receive audio multiplex switch (ISA/ISB) and then it passes to de-emphasis stages. The de-emphasized audio passes through the digital volume control, through an audio switch (RXO), and then out of the ASP at U804 pin 27.

Public Address Audio Path

The public address audio path is similar to the path of the normal mic audio from the MIC HI line (J701 pin 4) through the ASP to its output at U804 pin 60. At this point (TX_AU) the public address audio is routed to audio op amp U301.1 via FET switch Q340 which is on during public addresses. Microcontroller U701 turns Q340 on by switching the SW4 output of the ASP (U804 pin 14) high. The output of U301.1 is then sent to the external PA speaker via the Audio Amplifier Board. During public addresses, transistor Q803 is turned on to energize the relay in the PA kit. This relay switches the audio to the PA speaker.

DTMF ENCODER U803

DTMF (Dual-Tone Multi-Frequency) tones are generated by encoder U803. A 3.579545 MHz clock set by crystal Y801 runs only when a tone is being generated during transmit keying. The encoder's oscillator is disabled by software to prevent harmonic and other spurious RF signals from interfering with the receiver. When a software command to generate a tone is sent to U803, the clock oscillator recovers in less than 3 milliseconds.

The microcontroller serially communicates with the DTMF encoder on the IIC CLK and IIC DATA lines. The DTMF tones at the output (U803 pin 5) are sent to the receiver's audio path in the ASP (U804 pin 29) to provide DTMF sidetones. They are also sent to the TX audio path via U804 pin 73.

5-VOLT REGULATOR U801

Regulator U801 supplies 5 Vdc power to the logic and analog circuits on the board. The 8-Volt regulator on the RF Board supplies U801 with 8 Vdc input power via J702 pin 3.

Regulator U801 generates a reset signal at power-up and if its output falls out of regulation. U801 pin 5 stays low at power-up until the output rises above 4.75 Vdc. It will also switch low if the supply falls below 4.75 Vdc during radio operation. This reset signal is inverted by Q804 and applied to the modem's active high reset input at U702 pin 33. See the modem circuit analysis section entitled **"Reset Logic"** for complete details on the board's reset circuitry.

8-VOLT REGULATOR U805

Regulator U805 provides regulated 8 Vdc power to the op amps on the board. This supply is also used to pull-up the MIC_HI (S52) input. U805 is fed from the switch A+ power (SW_A+) line on J702 pin 6.

DUPLEX SIDETONE CANCELLATION

Duplex MDR radios employing a single VCO on the RF Board for transmit and receive operation use U302 and the associated circuits to provide sidetone delay and amplitude equalization when they are operating in duplex mode. These circuits allow the Audio/Logic Board to cancel the portion of the FM detected signal that is generated when the receiver's local oscillator (the VCO) is frequency modulated for the transmitter.

Potentiometer R361 provides a delay adjustment from approximately 150 to 300 microseconds of the TX_MOD signal at J702 pin 8. The delayed sidetone signal is fed back into the receive path through J2/P2, R359, C355 and R340 to the ASP (U804 pin 44). Potentiometer R359 provides amplitude adjustment from 0 to unity gain of the TX_MOD signal. The op amp in the ASP provides the summing amp configuration that cancels the detected VCO signal.

Jumper J2 and plug P2 configure the polarity of the sidetone to be fed back to the receiver summing amp in the ASP. If P2 is installed on J2 pins 1 and 2, the sidetone has the same polarity as the TX_MOD signal. If P2 is installed on J2 pins 2 and 3, then the sidetone has the negative polarity of the TX mod signal.

AEGIS INTERFACE AND RADIO DATA INTERFACE

Connector J910 provides interface of the digitally encrypted voice option on 800 MHz radios. This connector also allows connection of the RS-232C compatible data option to communicated with a host computer. When neither option is used, plugs P3 through P7 are installed onto J910 to loop signals between J701 and the circuitry on the Audio/Logic Board.

MULTIPLEXED CONTROL LINES

Several pins on connector J701 are multiplexed lines that are used in a different manner for the different radios and/or modes of operation.

MDX radios use J701 pin 2 as a PTT input; it is pulled low when the MDX microphone is keyed. In an MDR installation, J701 pin 2 is used as an external speaker mute control output; it is pulled low when the speaker audio is muted. J701 pin 2 is also the flash power input used for programming the flash memory in both the MDR and MDX radios. The radio is forced in the flash mode of operation when this line goes to 12 Vdc.

J701 pin 7 is the serial service request input for MDX radios. This pin is the handset speaker mute output for MDR radios.

J701 pins 1, 3, 6, and 7 provide RS-232C inputs and outputs for Data Radio applications.

AUDIO/LOGIC BOARD
19D903963G1
ISSUE 3

SYMBOL	PART NO.	DESCRIPTION
		CAPACITORS
C302	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C303 and C304	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C305	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C306	19A705205P223	Tantalum: 22 µF, 6 VDCW; sim to Sprague 293D.
C307	19A705205P19	Tantalum: 2.2 µF, 10 VDCW; sim to Spargue 293D.
C310	19A149896P121	Ceramic: .01 µF ±10%, 50 VDCW.
C340	19A702052P45	Ceramic: .22 µF ±5%, 16 VDCW.
C341	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C351 thru C354	19A702061P99	Ceramic: 1000 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C355	19A705205P223	Tantalum: 22 µF, 6 VDCW; sim to Sprague 293D.
C601	19A705205P19	Tantalum: 2.2 µF, 10 VDCW; sim to Spargue 293D.
C602	19A149896P121	Ceramic: .01 µF ±10%, 50 VDCW.
C603 and C604	19A149896P115	Ceramic: 3300 pF ±10%, 50 VDCW.
C605	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C607	19A149896P121	Ceramic: .01 µF ±10%, 50 VDCW.
C608	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C609	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C610	19A705205P223	Tantalum: 22 µF, 6 VDCW; sim to Sprague 293D.
C611	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C612	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C613 and C614	19A705205P19	Tantalum: 2.2 µF, 10 VDCW; sim to Spargue 293D
C615	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C623	19A149897P43	Ceramic: 150 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C624	19A149897P51	Ceramic: 330 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C630	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C635	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C636	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef0 ±30 PPM/°C.
C640	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C641	19A149897P55	Ceramic: 470 pF ±5%, 50 VDCW, temp coef0 30 PPM/°C.
C642	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C643 and C644	19A149896P109	Ceramic: 1000 pF ±10%, 50 VDCW.
C645	19A149896P115	Ceramic: 3300 pF ±10%, 50 VDCW.
C646	19A149896P117	Ceramic: 4700 pF ±10%, 50 VDCW.
C651	19A705205P223	Tantalum: 22 µF, 6 VDCW; sim to Sprague 293D.
C652	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C653	19A702052P45	Ceramic: 0.22 µF ±10%, 16 VDCW.
C654	19A149897P31	Ceramic: 47 pF ±5%, 50 VDCW, temp coef0 ±30 PPM/°C.
C655	19A149896P109	Ceramic: 1000 pF ±10%, 50 VDCW.
C656	19A149897P39	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
*C701	19A149897P15	Ceramic: 3300 pF ±5%, 50 VDCW.
C702 thru C708	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 30 PPM/°C.
C720	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 30 PPM/°C.
C725 and C726	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 30 PPM/°C.
C727 thru C729	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C730	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C731	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C732 and C733	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C734	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C735	19A149897P21	Ceramic: 18 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C736 and C737	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C738	19A149897P15	Ceramic: 10 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C739	19A149897P27	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C740 thru C742	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C744 and C749	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C750	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C751 thru C753	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C754	19A149897P27	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C780	19A149897P27	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C801	19A705205P19	Tantalum: 2.2 µF, 10 VDCW; sim to Spargue 293D.
C802 and C803	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C805	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C808	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C809	19A705205P223	Tantalum: 22 µF, 6 VDCW; sim to Sprague 293D.
C810 thru C815	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C817	19A149897P47	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C820	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C870	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C871	19A149897P27	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C901 thru C914	19A149897P27	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C915 thru C919	19A149897P39	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C920	19A149897P55	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C921 and C922	19A149897P39	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
		DIODES
D701 thru D706	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
D710	19A705377P5	Silicon, Hot Carrier:á sim to HSMS-2804.
		JACKS
J1 and J2	19A704852P2	Connector: 3-pin male header.
J701	19B209727P61	Connector: 9-contact D-type, right angle mounting; sim to AMP 747840-2.
J702	19A704779P11	Connector: sim to Molex 22-17-2122.
J910	19A702333P57	Connector: 32-contact dual-row header.
		PLUGS
P1 thru P7	19A702104P3	Connector: 2-position shorting; sim to Dupont 68786-202.
		TRANSISTORS
Q340 and Q342	344A4183P1	Silicon, N-Channel FET: sim to MMBF5484LT1.
Q601	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q602	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q603	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q604	19A705945P2	Silicon, Dual NPN: sim to R OHM IMX3.
Q605	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q606	19A703197P2	Silicon, PNP: sim to MMBT4403, low profile.
Q607	19A702503P3	Silicon, NPN: sim to MMBT4401.
Q640	344A4183P1	Silicon, N-Channel FET: sim to MMBF5484LT1.
Q701 and Q702	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q801	19A700076	P2Silicon, NPN: sim to MMBT3904, low profile.
Q802	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q803	19A702503P3	Silicon, NPN: sim to MMBT4401.
Q804	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q805 and Q807	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		RESISTORS
R301	19A149818P153	Metal film: 15K ohms ±5%, 1/16 w.
R304	19A149818P333	Metal film: 33K ohms ±5%, 1/16 w.
R305	19A149818P272	Metal film: 2.7K ohms ±5%, 1/16 w.
R309	19A149818P153	Metal film: 15K ohms ±5%, 1/16 w.
R315	19B800607P561	Metal film: 560 ohms ±5%, 1/8 w.
R316	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R318	19A149818P682	Metal film: 6.8K ohms ±5%, 1/16 w.
R317	19A149818P472	Metal film: 4.7K ohms ±5%, 1/16 w.
R340	19A149818P472	Metal film: 4.7K ohms ±5%, 1/16 w.
R341	19A149818P562	Metal film: 5.6K ohms ±5%, 1/16 w.
R342 and R343	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R344	19A149818P105	Metal film: 1M ohms ±5%, 1/16 w.
R351	19A702931P356	Metal film: 37.4K ohms ±1%, 1/8 w.
R352	19A702931P374	Metal film: 57.6K ohms ±1%, 1/8 w.
R353	19A702931P335	Metal film: 22.6K ohms ±1%, 1/8 w.
R354	19A702931P374	Metal film: 57.6K ohms ±1%, 1/8 w.
R355	19A702931P340	Metal film: 25.5K ohms ±1%, 1/8 w.
R356	19A702931P361	Metal film: 42.2K ohms ±1%, 1/8 w.
R357 and R358	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R359	19B800779P14	Variable: 47K ohms, ±25%, 3 watt.
R360	19A702931P361	Metal film: 42.2K ohms ±1%, 1/8 w.
R361	19B800779P14	Variable: 47K ohms, ±25%, 3 watt.
R362	19A702931P361	Metal film: 42.2K ohms ±1%, 1/8 w.
R365	19A149818P682	Metal film: 6.8K ohms ±5%, 1/16 w.
R366	19A149818P472	Metal film: 4.7K ohms ±5%, 1/16 w.
R601	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R602	19A149818P102	Metal film: 1K ohms ±5%, 1/16 w.
R603	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R604	344A3304P1001	Metal film: 1K ohms ±1%, 1/10 w.
R605	19A149818P823	Metal film: 82K ohms ±5%, 1/16 w.
R607	344A3304P2493	Metal film: 249K ohms ±1%, 1/10 w.
R608	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R609	19A149818P393	Metal film: 39K ohms ±5%, 1/16 w.
R610	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R611 and R612	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R613	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R614	19A149818P153	Metal film: 15K ohms ±5%, 1/16 w.
R615 and R616	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R617	19A149818P153	Metal film: 15K ohms ±5%, 1/16 w.
R618 and R619	19A149818P103	Metal film:10K ohms ±5%, 1/16 w.
R620	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R622	19A149818P393	Metal film: 39K ohms ±5%, 1/16 w.
R623 and R624	19A149818P333	Metal film: 33K ohms ±5%, 1/16 w.
R625	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.

* COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NO.	DESCRIPTION
R626	19A149818P272	Metal film: 2.7K ohms ±5%, 1/16 w.
R627 and R628	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R630	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R632	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R633	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R634	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R635	19A149818P682	Metal film: 6.8K ohms ±5%, 1/16 w.
R636	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R637	19A149818P105	Metal film: 1M ohms ±5%, 1/16 w.
R640	19A149818P152	Metal film: 1.5K ohms ±5%, 1/16 w.
R641	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R643	19A149818P105	Metal film: 1M ohms ±5%, 1/16 w.
R644	19A149818P472	Metal film: 4.7K ohms ±5%, 1/16 w.
R645	19A149818P105	Metal film: 1M ohms ±5%, 1/16 w.
R651 and R652	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R653	19A149818P274	Metal film: 270K ohms ±5%, 1/16 w.
R654	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R655	19A149818P274	Metal film: 270K ohms ±5%, 1/16 w.
R656	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R657 and R658	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R659	19A149818P153	Metal film: 15K ohms ±5%, 1/16 w.
R660	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R661	344A3304P1002	Metal film: 10K ohms ±1%, 1/10 w.
R662	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R663	344A3304P3483	Metal film: 348K ohms ±1%, 1/10 w.
R664	19A149818P684	Metal film: 680K ohms ±5%, 1/16 w.
R702 thru R706	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R707	19A149818P470	Metal film: 47 ohms ±5%, 1/16 w.
R708	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R725	19A149818P100	Metal film: 10 ohms ±5%, 1/16 w.
R726	19A149818P153	Metal film: 15K ohms ±5%, 1/16 w.
R727	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R728	19A149818P472	Metal film:4.7K ohms ±5%, 1/16 w.
R72 thru R732	919A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R733 and R734	19A149818P333	Metal film: 33K ohms ±5%, 1/16 w.
R735	19A149818P332	Metal film: 3.3K ohms ±5%, 1/16 w.
R736 thru R739	19A149818P100	Metal film: 10 ohms ±5%, 1/16 w.
R740	19A149818P561	Metal film: 560 ohms ±5%, 1/16 w.
R741	19A149818P333	Metal film: 33K ohms ±5%, 1/16 w.
R742	19A149818P823	Metal film: 82K ohms ±5%, 1/16 w.
R743	19A149818P101	Metal film:100 ohms ±5%, 1/16 w.
R745 thru R751	19A149818P561	Metal film:560 ohms ±5%, 1/16 w.

SYMBOL	PART NO.	DESCRIPTION
R752	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R753	19A149818P562	Metal film: 5.6K ohms ±5%, 1/16 w.
R760	19A149818P682	Metal film: 6.8K ohms ±5%, 1/16 w.
R770	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R773	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R774	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R780	19A149818P392	Metal film: 3.9K ohms ±5%, 1/16 w.
R801	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R802	19A149818P102	Metal film: 1K ohms ±5%, 1/16 w.
R806 and R807	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R808	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R809	19A149818P100	Metal film: 10 ohms ±5%, 1/16 w.
R810	19A149818P470	Metal film: 47 ohms ±5%, 1/16 w.
R825	19A149818P184	Metal film: 180K ohms ±5%, 1/16 w.
R826	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R827	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R828	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R839	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R840	19A149818P182	Metal film: 1.8K ohms ±5%, 1/16 w.
R841	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R842	19A149818P0R0	Jumper.
R843 and R844	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R846	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R848 and R849	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R850	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R852	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R860	19A149818P105	Metal film: 1megohms ±5%, 1/16 w.
R861	19A149818P272	Metal film: 2.7K ohms ±5%, 1/16 w.
R871	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R890 and R891	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R901 thru R914	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
R915	19A149818P182	Metal film: 1.8K ohms ±5%, 1/16 w.
R916	19A149818P101	Metal film: 100 ohms ±5%, 1/16 w.
		THERMISTOR
RT601	19A705813P2	Thermistor: sim to AL03006-58.2K-97-G100.
		INTEGRATED CIRCUITS
U301 and U302	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U601	19A702293P3	Linear: Dual Op Amp; sim to LM3580.
U602	344A3999P201	Linear: Notch Filter; sim to LMF90CC.
U701	344A4014P10	Digital: 8-Bit Microcontroller; sim to N83C51GB.
U702	19A704727P6	Digital: Modem.
U703	344A4029P201	Digital: 128K x 8-Bit Flash EEPROM; sim to E28F001BX-T120.

SYMBOL	PART NO.	DESCRIPTION
U706	RYT1186063/1	Digital: 48-Bit Serial Number ROM; sim to DS2400Z.
U707	19A705603P6	Digital: 8K x 8-Bit CMOS RAM; sim to Hyundai HY6264ALJ-10.
U708	19A703483P302	Digital: Quad 2-Input NAND Gate; sim to 74HC00.
U801	344A3202P201	Linear: Voltage Regulator; sim to LP2951ACM.
U802	19A149755P5	Digital: 8K x 8-Bit EEPROM; sim to 28C64.
U803	344A3800P102	Linear: Tone Generator; sim to PCD3312C.
U80	4344A3291P1	Audio Signal Processor; sim to MB87780PFV-G-BND.
U805	19A704971P11	Linear: 8-Volt Regulator; sim to MC78LO8ACD.
		VOLTAGE REGULATORS
VR802	344A3384P20	Silicon: 20-Volt Zener; sim to 1SBM5932A.
		CRYSTALS
Y601	344A4261G2	Crystal, resonator: 613.5 kHz.
Y602	344A4261G1	Crystal, resonator: 586.5 kHz.
Y701	19A702511G64	Crystal: 11.0592 MHz.
Y801	19A702511G65	Crystal: 3.579545 MHz.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

REV. A - AUDIO/LOGIC BOARD 19D903963G1
REV. B - AUDIO/LOGIC BOARD 19D903963G1

Incorporated in initial shipments.

REV. C - AUDIO/LOGIC BOARD 19D903963G1

Changes gain of Vol/Sq. Hi into squelch high pass filter.
R614 was 47K ohms (19A149818P473).

REV. D - AUDIO/LOGIC BOARD 19D903963G1

Correct busy tone notch failure at high temperatures
Q607 was 19A700236P4.
R627 and R628 were 6.8K ohms (19A149818P682).
R743 was 560 ohms (19A149818P561).

REV. E - AUDIO/LOGIC BOARD 19D903963G1

Prevent flash memory dump and change op-amp for lower DC bias for busy tone decoding.
U601 was 19A116297P7.
Q607 was 19A700236P4.
C340 was 0.1 µF (19A702052P134).
R626 was 4.7K ohms (19A149818P472).
R728 was 6.8K ohms (19A149818P682).
R770 was 560 ohms (19A149818P561).
Q807, Q342, R860, R861, R890 and R891 were added.

REV. F - AUDIO/LOGIC BOARD 19D903963G1

Improves busy tone notch oscillator stability.
C623 was 220 pF (19A149818P47).
C624 was 470 pF (19A149897P55).

REV. G - AUDIO/LOGIC BOARD 19D903963G1

Part no longer available.
U706 was 344A405050P101.

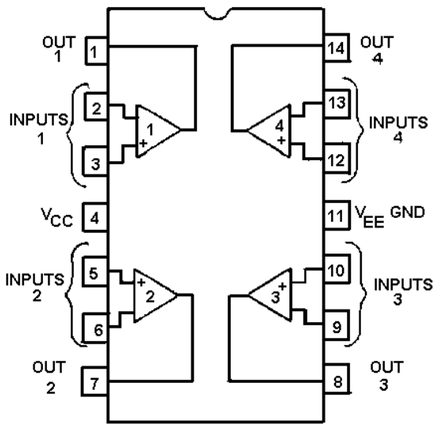
REV. H - AUDIO/LOGIC BOARD 19D903963G1

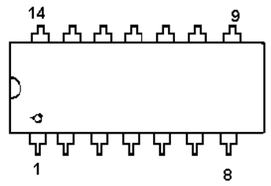
Eliminates micro clock noise.
C701 was 470 pF (19A149897P55).

REV. J - AUDIO/LOGIC BOARD 19D903963G1

Eliminates micro clock noise.
C701 was 2200 pF (19A149896P13).
C606 (19A149896P117) and R621 (19A149818P474) were deleted.

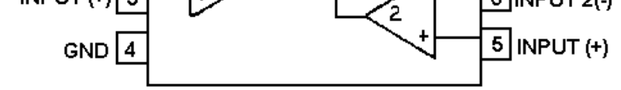
PIN CONNECTIONS





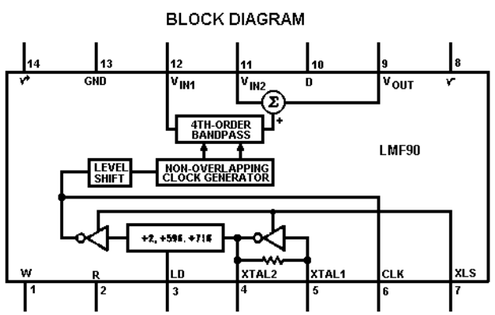
U301 & U302 QUAD OP AMPS
19A704883P2

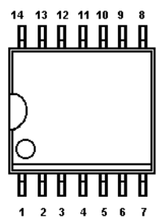
PIN CONNECTIONS



U601 DUAL OP AMP
19A702293P3

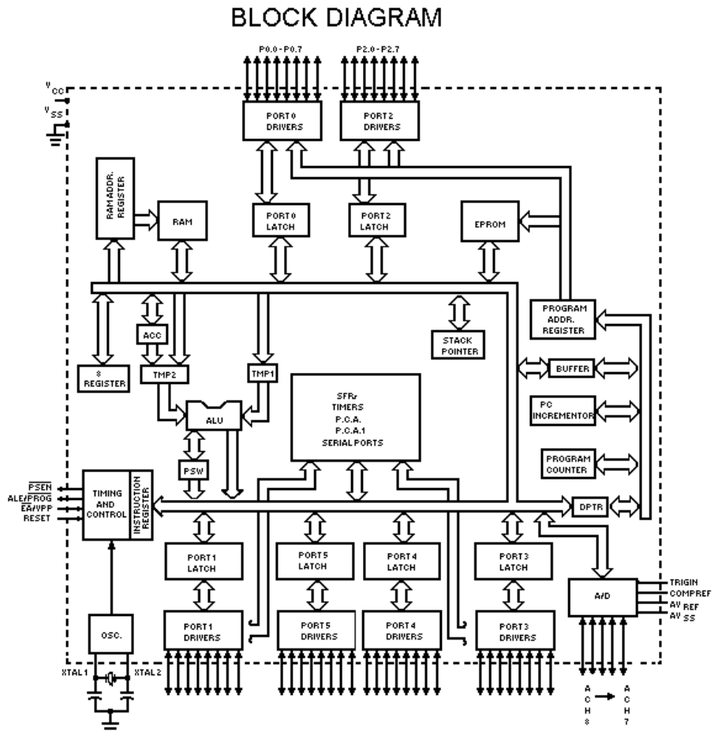
BLOCK DIAGRAM

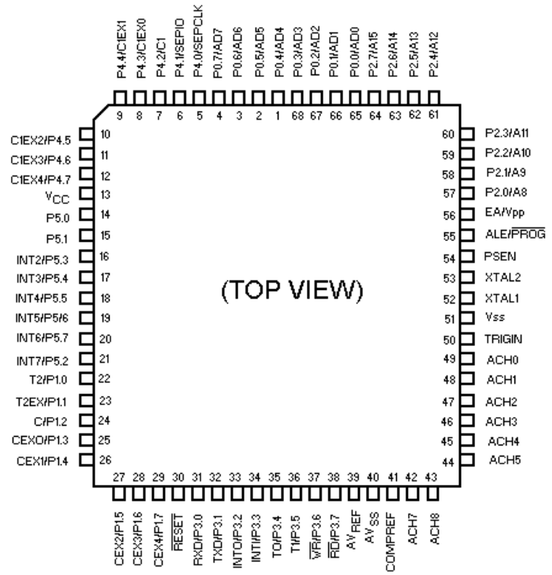




U602 NOTCH FILTER
344A3999P201

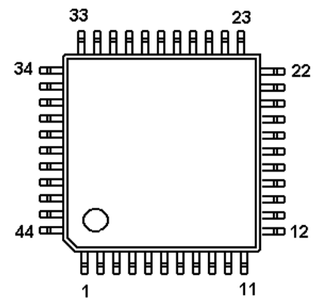
BLOCK DIAGRAM

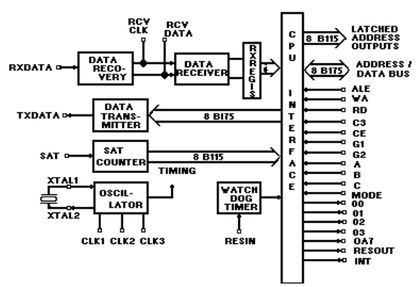




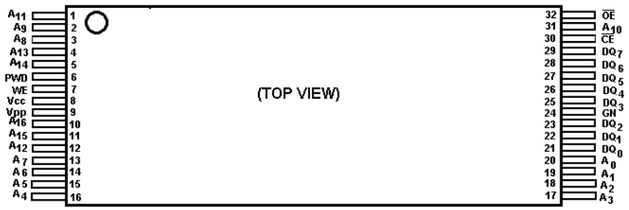
U701 8-BIT MICROCONTROLLER
344A401P10

PIN NAME	44 PACK PIN	DESCRIPTION
RE	39	READ ENABLE (ACTIVE LOW)
EN	41	CHIP ENABLE (ACTIVE LOW)
RESOUT	43	RESET OUTPUT (ACTIVE HIGH)
AD0	44	BI-DIRECTIONAL ADDRESS / DATA BUS
AD1	1	BI-DIRECTIONAL ADDRESS / DATA BUS
AD2	2	BI-DIRECTIONAL ADDRESS / DATA BUS
AD3	4	BI-DIRECTIONAL ADDRESS / DATA BUS
AD4	6	BI-DIRECTIONAL ADDRESS / DATA BUS
AD5	8	BI-DIRECTIONAL ADDRESS / DATA BUS
AD6	10	BI-DIRECTIONAL ADDRESS / DATA BUS
AD7	11	BI-DIRECTIONAL ADDRESS / DATA BUS
ALE	12	ADDRESS LATCH ENABLE (ACTIVE HIGH)
VSS	13	GROUND
CLK1	15	BUFFERED OSCILLATOR OUTPUT
VDD	17	POWER SUPPLY
XTAL1	19	OSCILLATOR INPUT
XTAL2	21	OSCILLATOR OUTPUT
CLK2	22	640 KHZ OUTPUT
DATAIN	2	RECEIVED DATA INPUT
SAT/G1	24	RECEIVED SAT INPUT/G1 EN. HC138 (ACT. HI)
TXDAT	26	TRANSMIT DATA OUTPUT
RCVCLK/Q2	28	RECOVERED CLOCK OUTPUT/Q2 OUTPUT FOR HC138
RCVDAT/Q0	30	RECOVERED DATA OUTPUT/Q0 OUTPUT FOR HC138
INT	32	INTERRUPT REQUEST (ACTIVE LOW O.D.)
RESIN	33	RESET INPUT (ACTIVE HIGH)
CS	34	CHIP SELECT (ACTIVE LOW)
CLK3/4	35	TRANSMIT CLOCK OUTPUT/CLK 1/6 OUTPUT
WR	37	WRITE ENABLE (ACTIVE LOW
MODE	18	Enable 44 pin fnactions (active low)
A	38	A input for HC138
B	36	B input for HC138
C	31	C input for HC138
G2B	20	G2B enable for HC138 (active low)
A0	40	A0 address output
A1	42	A1 address output
A2	3	A2 address output
A3	5	A3 address output
A4	7	A4 address output
A5	9	A5 address output
A6	14	A6 address output
A7	16	A7 address output
Q1	29	Q1 output for HC138
Q3	27	Q3 output for HC138
Q47	25	Q4 - Q7 (ored internally) output for HC138

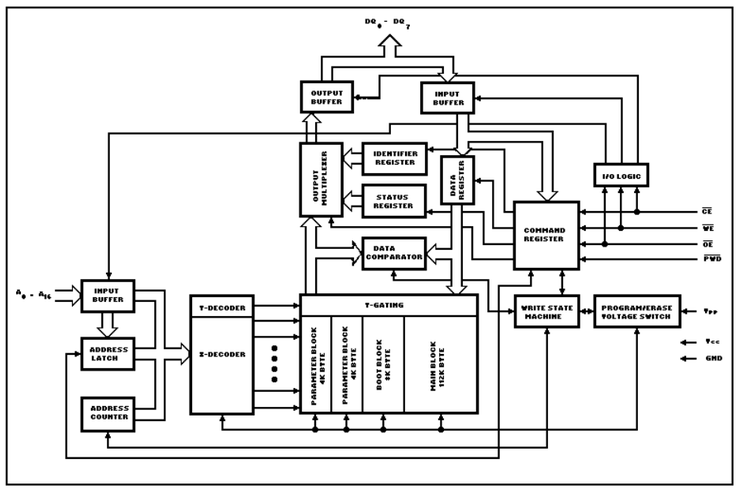




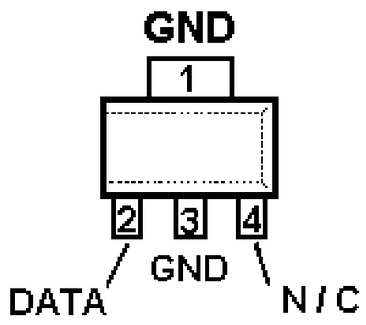
U702 MODEM
19A704727P6



BLOCK DIAGRAM

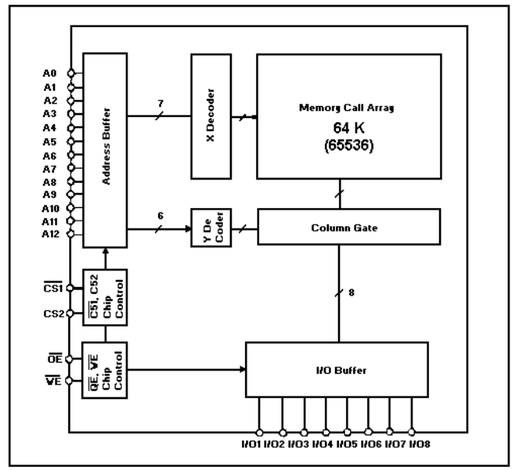


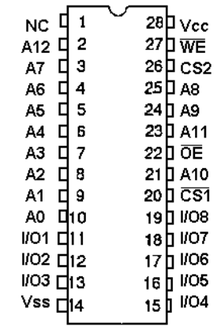
U703 128K x 8-BIT FLASH EEPROM
344A4029P201



U706 48-BIT SERIAL NUMBER ROM
RYT1186063/1

BLOCK DIAGRAM



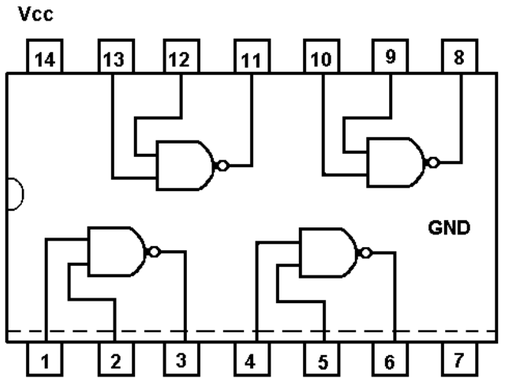


TRUTH TABLE

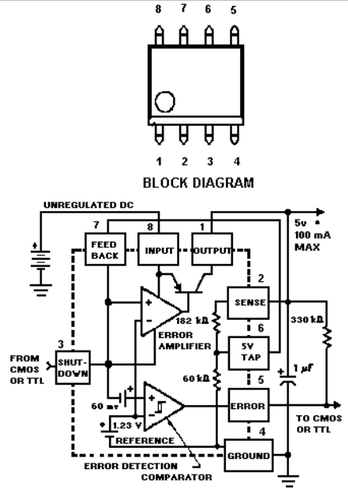
$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	Mode
X	H	X	X	Not Selected (Power Down)
X	X	L	X	
H	L	H	H	Output Disabled
H	L	H	L	Read
L	L	H	H	Write
L	L	H	L	

X: H or L

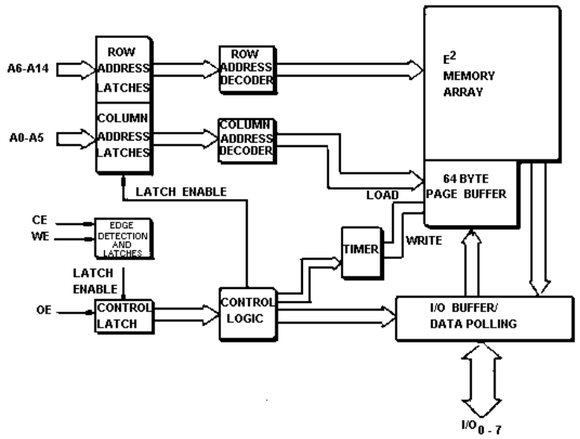
U707 8K x 8-BIT CMOS RAM
19A705603P6



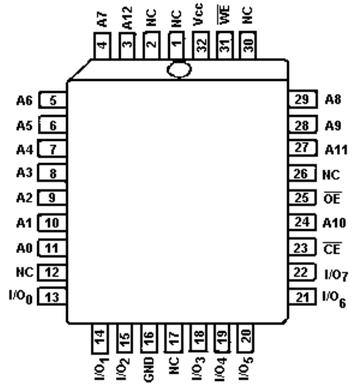
U708 QUAD 2-INPUT NAND GATE
19A703483P302



U801 VOLTAGE REGULATOR
344A3202P201

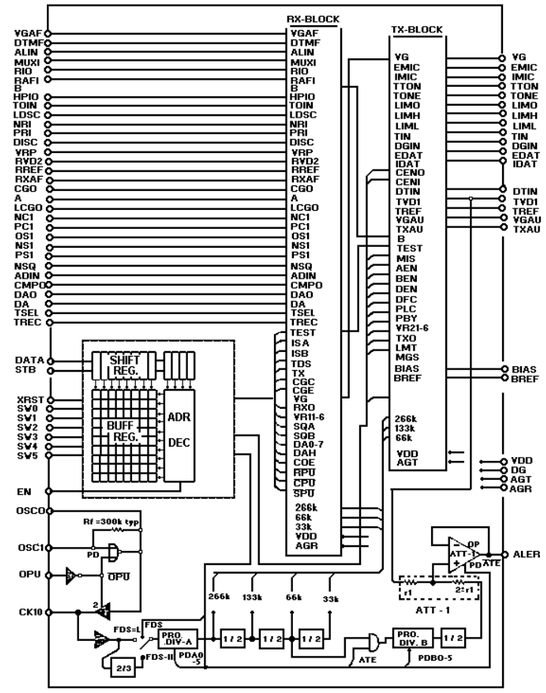


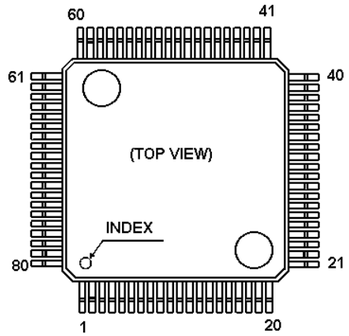
PLASTIC LEADED CHIP CARRIER
TOP VIEW



U802 8K X 8-BIT EEPROM
19A149755P5

BLOCK DIAGRAM



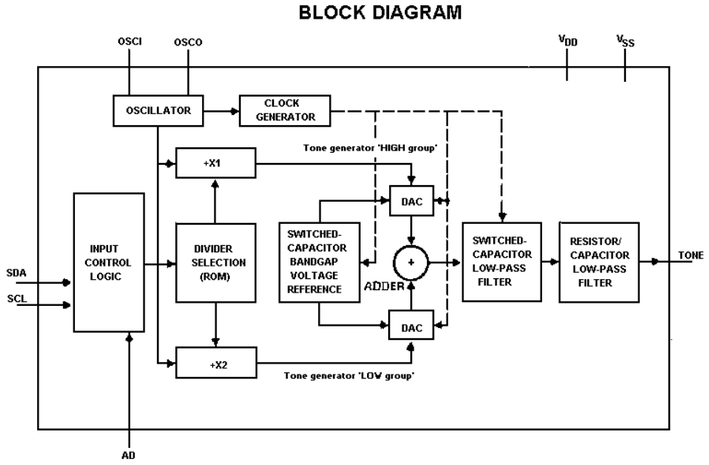


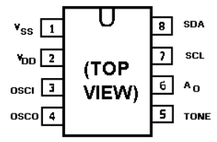
PIN NAME TABLE

No	IO	name	No	IO	name	No	IO	name	No	IO	name
1	---	NC	21	O	LDSC	41	G	AGR	61	---	NC
2	I	OPU	22	O	LCGO	42	AO	MUXI	62	G	AGT
3	G	DG	23	O	CMPO	43	AO	R10	63	AO	TVD2
4	I	OSCI	24	---	NC	44	AI	RAFI	64	AO	TREF
5	O	OSCO	25	I	TSEL	45	AO	HP10	65	AO	BIAS
6	IO	CK10	26	VD	VDD	46	AI	VRP	66	AO	BREF
7	G	DG	27	AO	RXAF	47	AO	DA	67	AO	LIMH
8	VD	VDD	28	AI	VGAF	48	AO	DAO	68	AO	LIML
9	I	XRST	29	AI	DTMF	49	AI	ADIN	69	AO	LIMO
10	I	EN	30	AI	ALIN	50	AI	DISC	70	AO	TONE
11	I	STB	31	AI	NR1	51	IO	TREC	71	---	NC
12	I	DATA	32	AI	PR1	52	AO	NSQ	72	AO	VGAU
13	O	SW5	33	---	NC	53	AO	OS1	73	AI	EMIC
14	O	SW4	34	AI	NC1	54	AI	NS1	74	AI	IMIC
15	O	SW3	35	AI	PC1	55	AI	PS1	75	AI	TTON
16	O	SW2	36	AO	A	56	---	NC	76	AO	ALER
17	O	SW1	37	AO	CGO	57	AI	TIN	77	VD	VDD
18	O	SW0	38	AI	TOIN	58	AI	CGIN	78	I	VG
19	VD	VDD	39	AO	RREF	59	AI	DTIN	79	I	EDAT
20	G	DG	40	AO	RVD2	60	AO	TXAU	80	I	IDAT

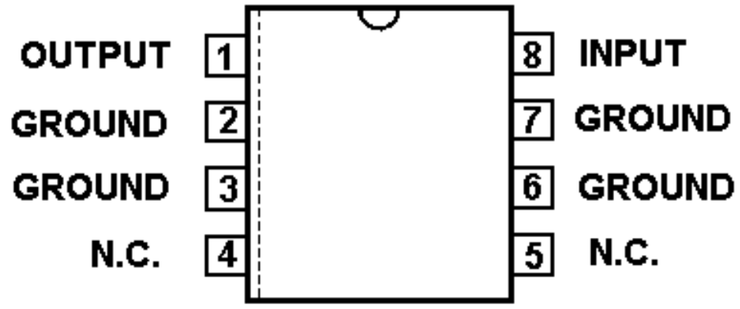
U804 AUDIO SIGNAL PROCESSOR
344A3291P1

BLOCK DIAGRAM





U803 TONE GENERATOR
344A3800P102



U805 8-VOLT REGULATOR
19A704971P11

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NOTES:

4. JUMPER CONFIGURATION

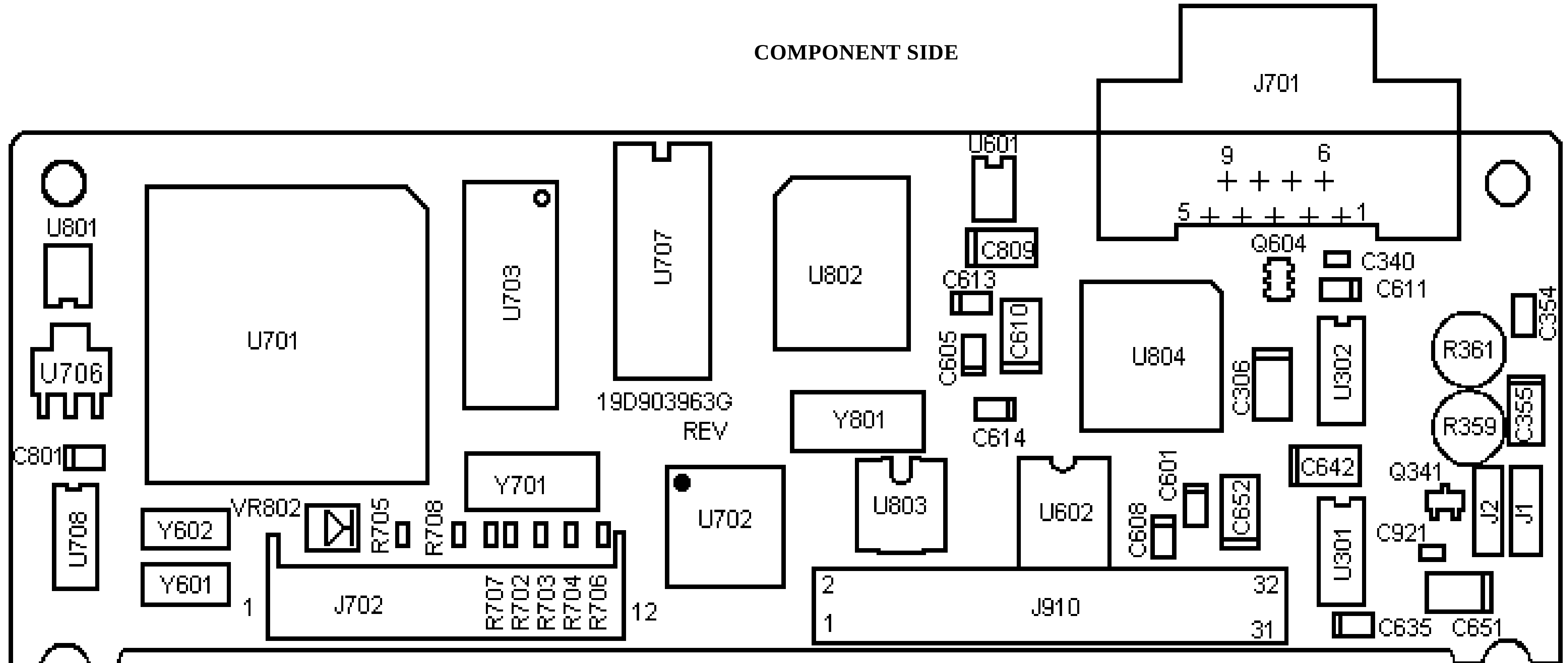
JUMPER	POSITION	NOTES
P1	J1-1 & 2	BASS BOOST DISABLED
	J1-2 & 3	BASS BOOST ENABLED
P2	J2-1 & 2	TX SIDETONE POSITIVE POLARITY
	J2-2 & 3	TX SIDETONE NEGATIVE POLARITY

FOR BOARD BUILD: INSTALL P1 ON J1-1 & 2
INSTALL P2 ON J2-2 & 3

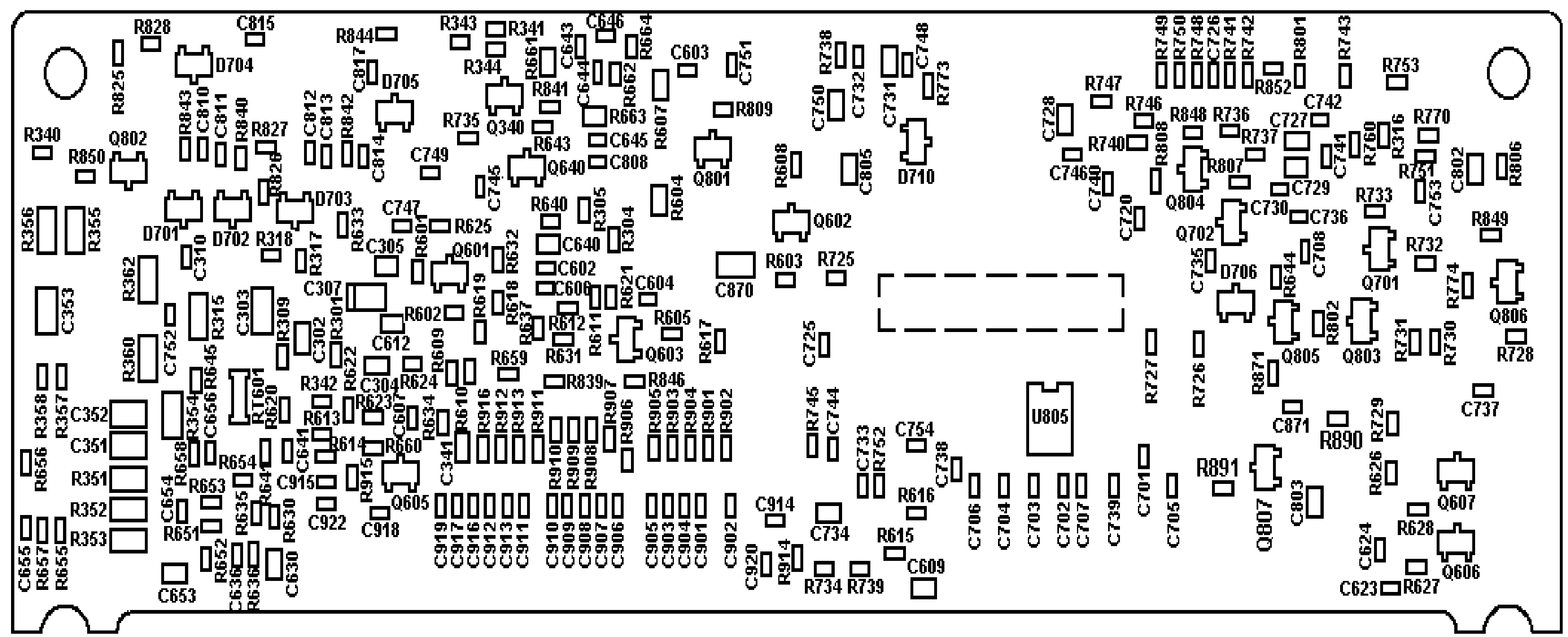
6. THE FOLLOWING ARE MOS DEVICES REQUIRING SPECIAL CARE PER 19A701294: U701 - U703, U707, 078, U802, & U804.

7. INSTALL: P3 ON J910 - 23, 24
P4 ON J910 - 25, 26
P5 ON J910 - 27, 28
P6 ON J910 - 29, 30
P7 ON J910 - 31, 32

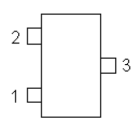
COMPONENT SIDE



SOLDER SIDE

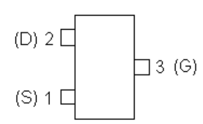


LEAD IDENTIFICATION FOR D701 - D706, & D710



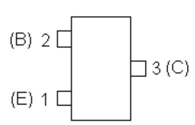
TOP VIEW

LEAD IDENTIFICATION FOR Q340, Q341, & Q640



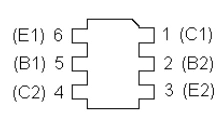
TOP VIEW

LEAD IDENTIFICATION FOR Q601 - Q603, Q605 - Q607, Q701 Q702, Q801 - Q806.



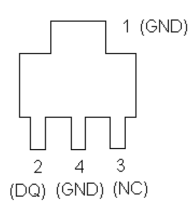
TOP VIEW

LEAD IDENTIFICATION FOR Q604



TOP VIEW

LEAD IDENTIFICATION FOR U706

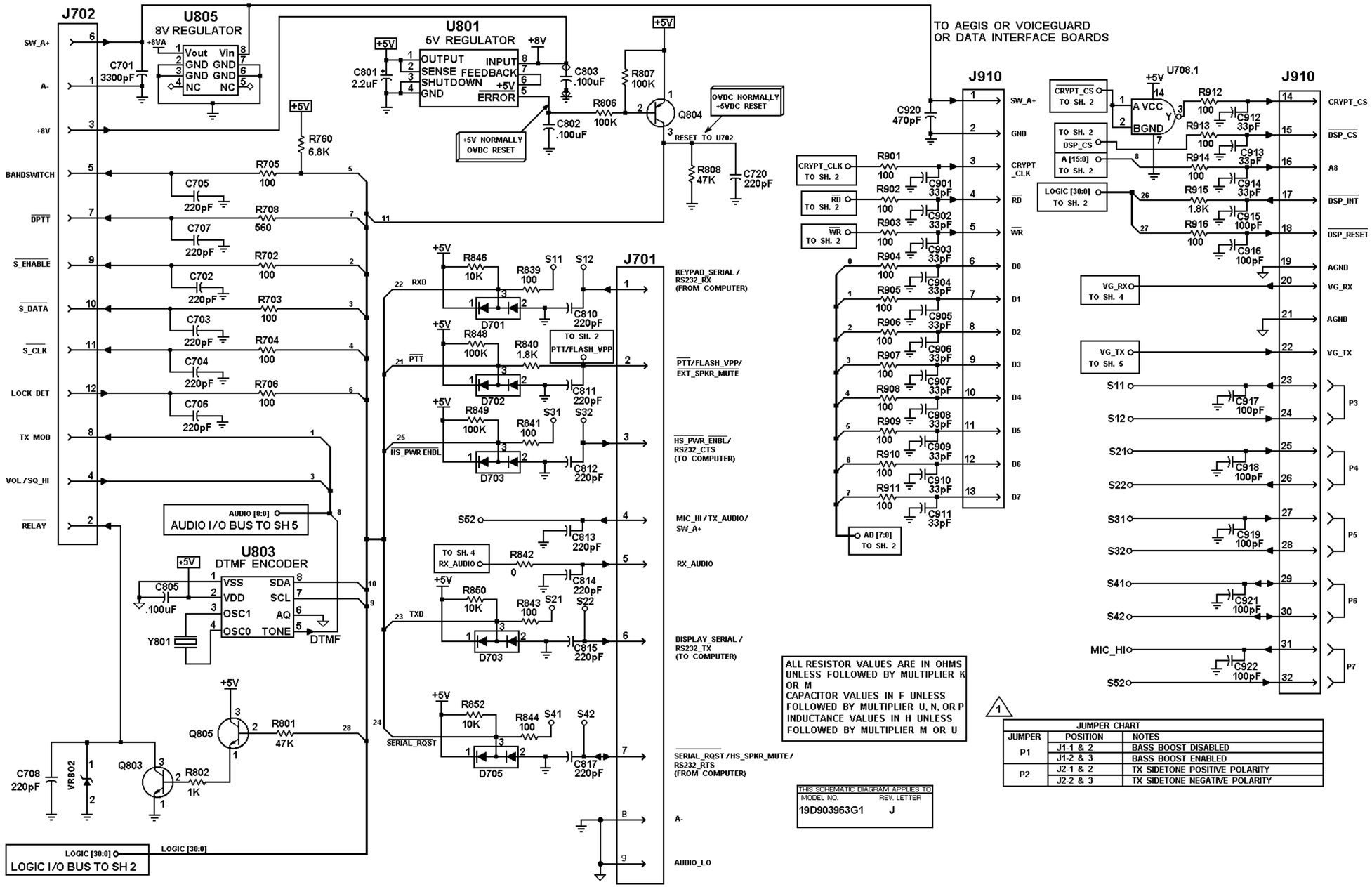


TOP VIEW

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

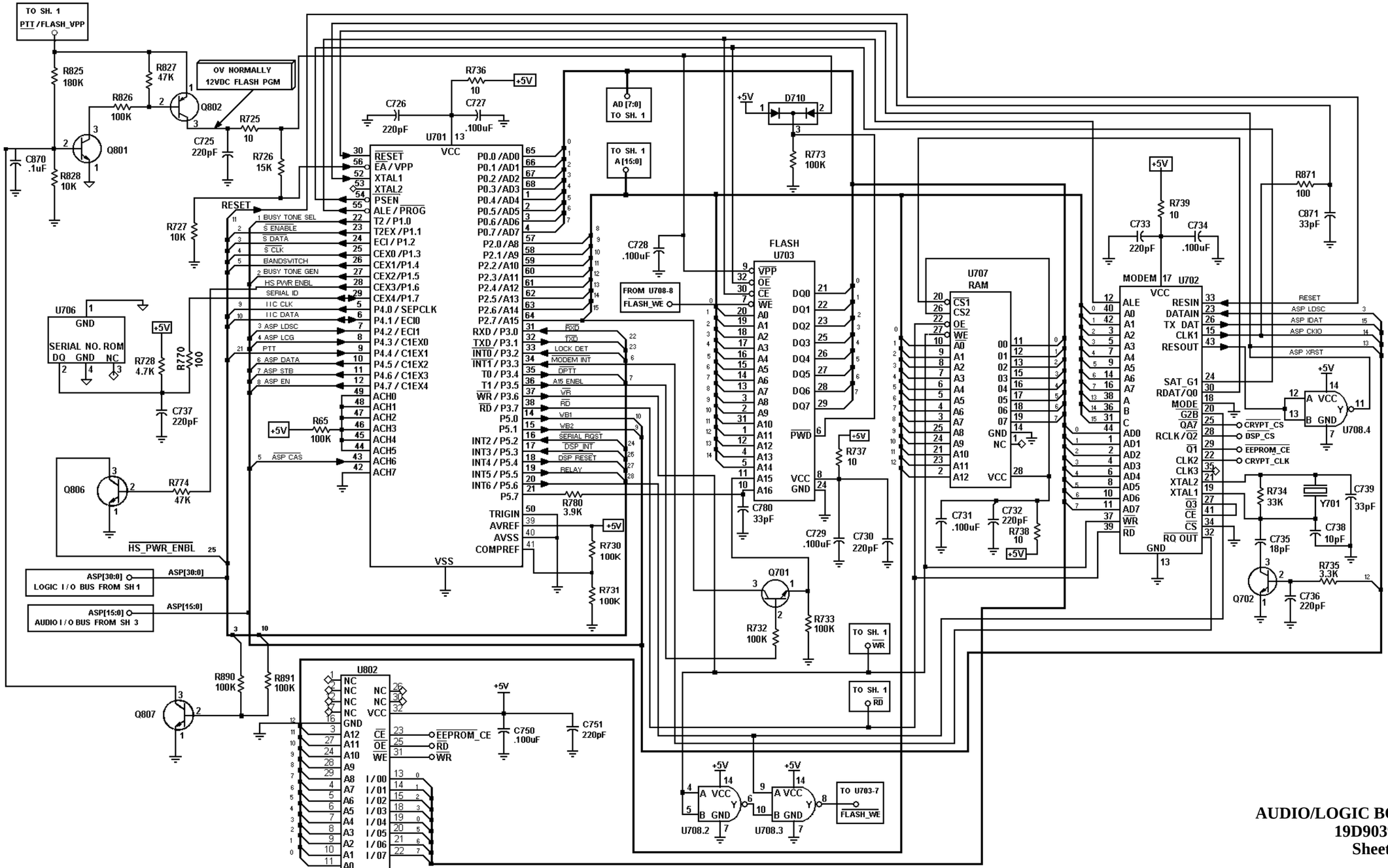
AUDIO/LOGIC BOARD 19D903963G1

(19D903963, Sh. 1, Rev. 10)



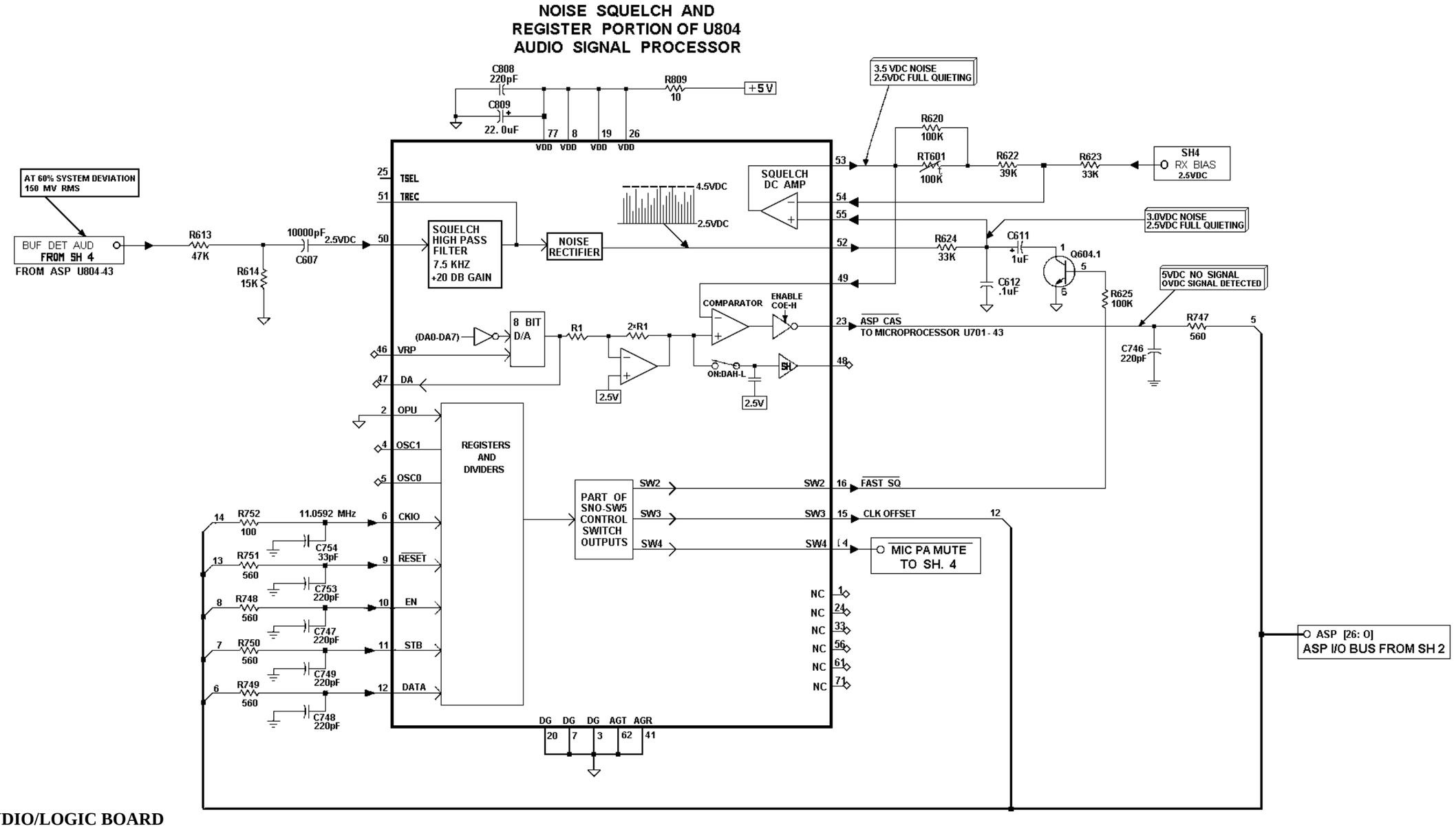
AUDIO/LOGIC BOARD
19D903963G1
Sheet 1 of 6

(19D904338, Sh. 1, Rev. 9)



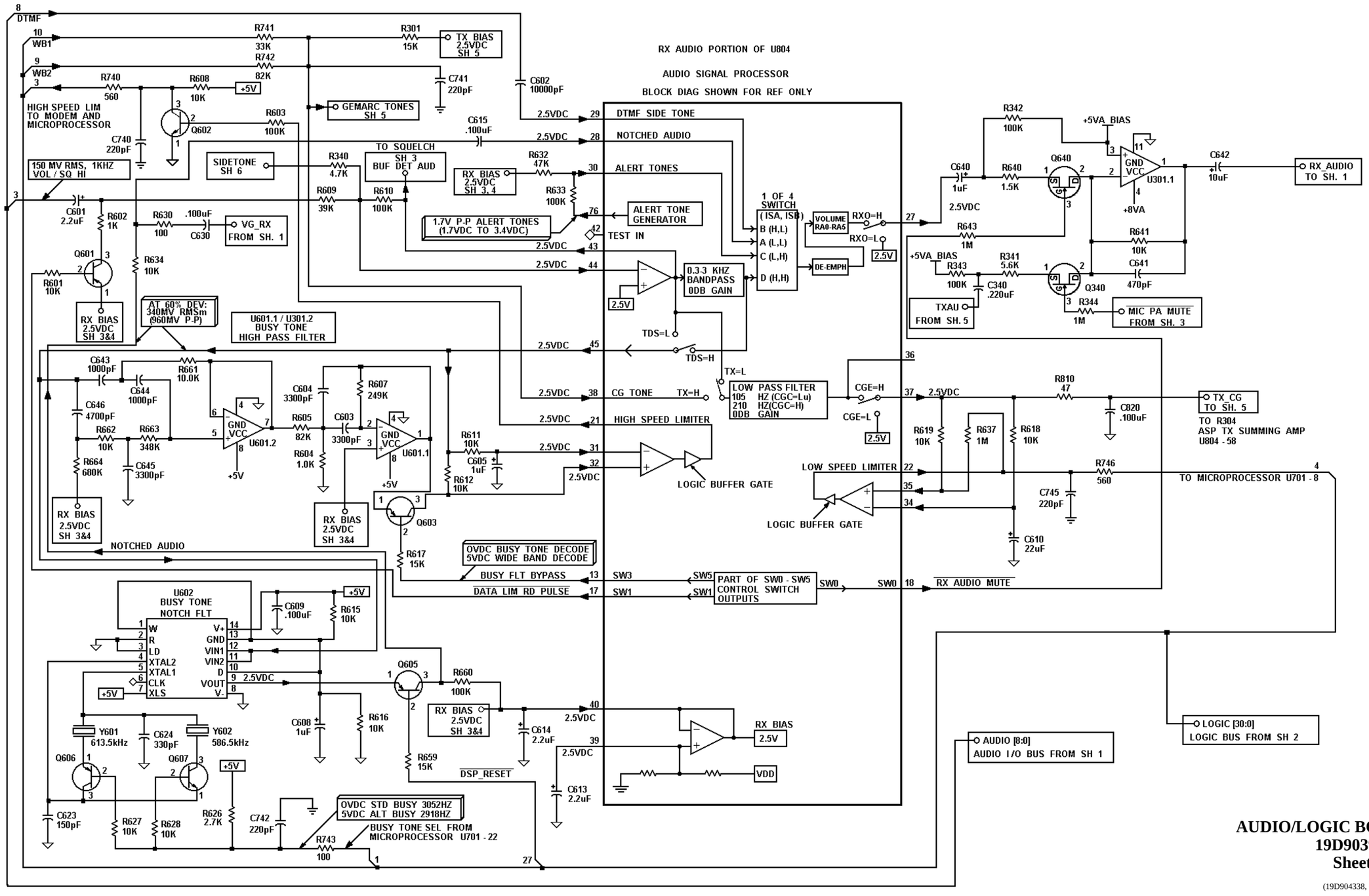
AUDIO/LOGIC BOARD
19D903963G1
Sheet 2 of 6

(19D904338, Sh. 2, Rev. 9)



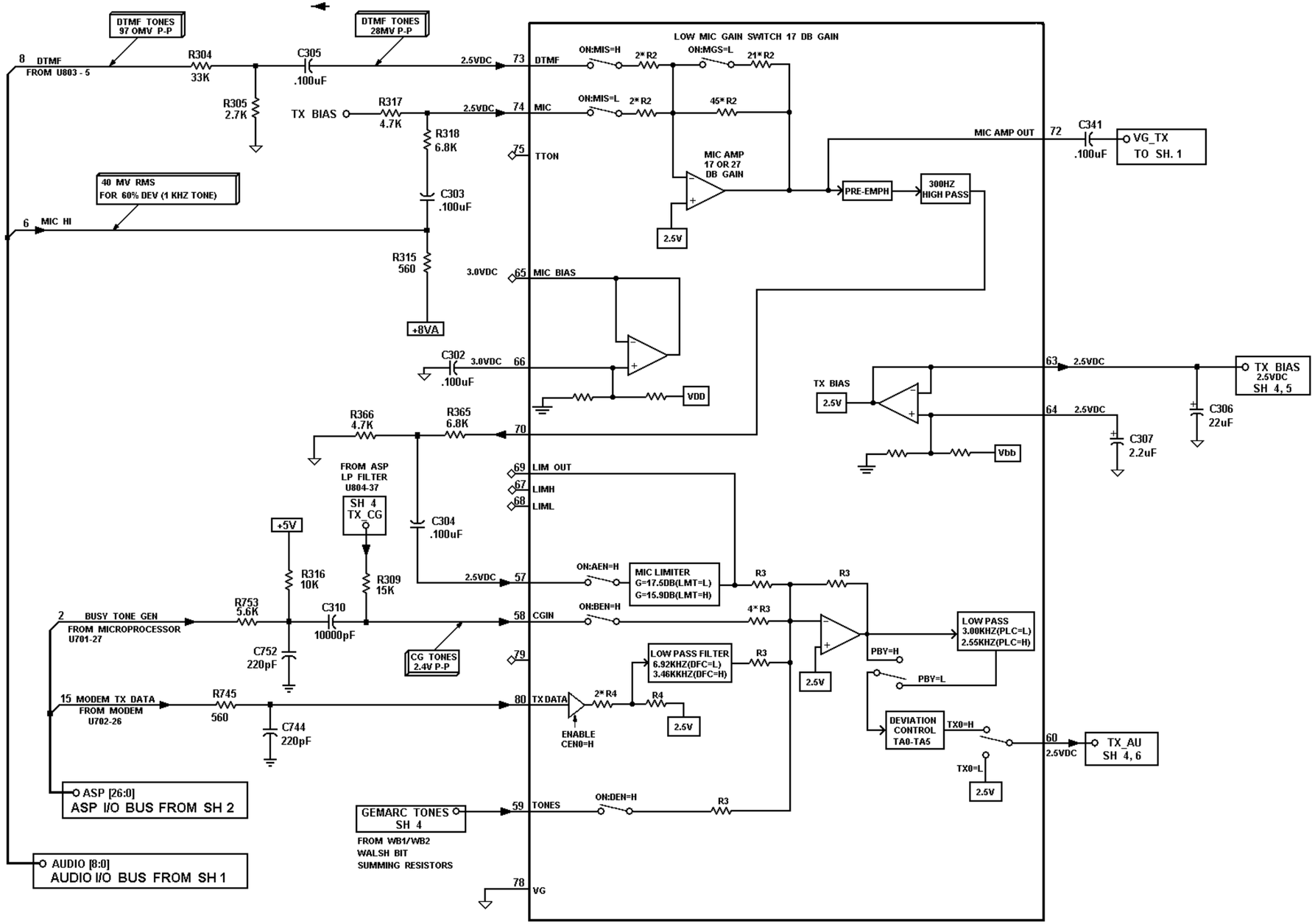
AUDIO/LOGIC BOARD
19D903963G1
Sheet 3 of 6

(19D904338, Sh. 3, Rev. 9)



AUDIO/LOGIC BOARD
19D903963G1
Sheet 4 of 6

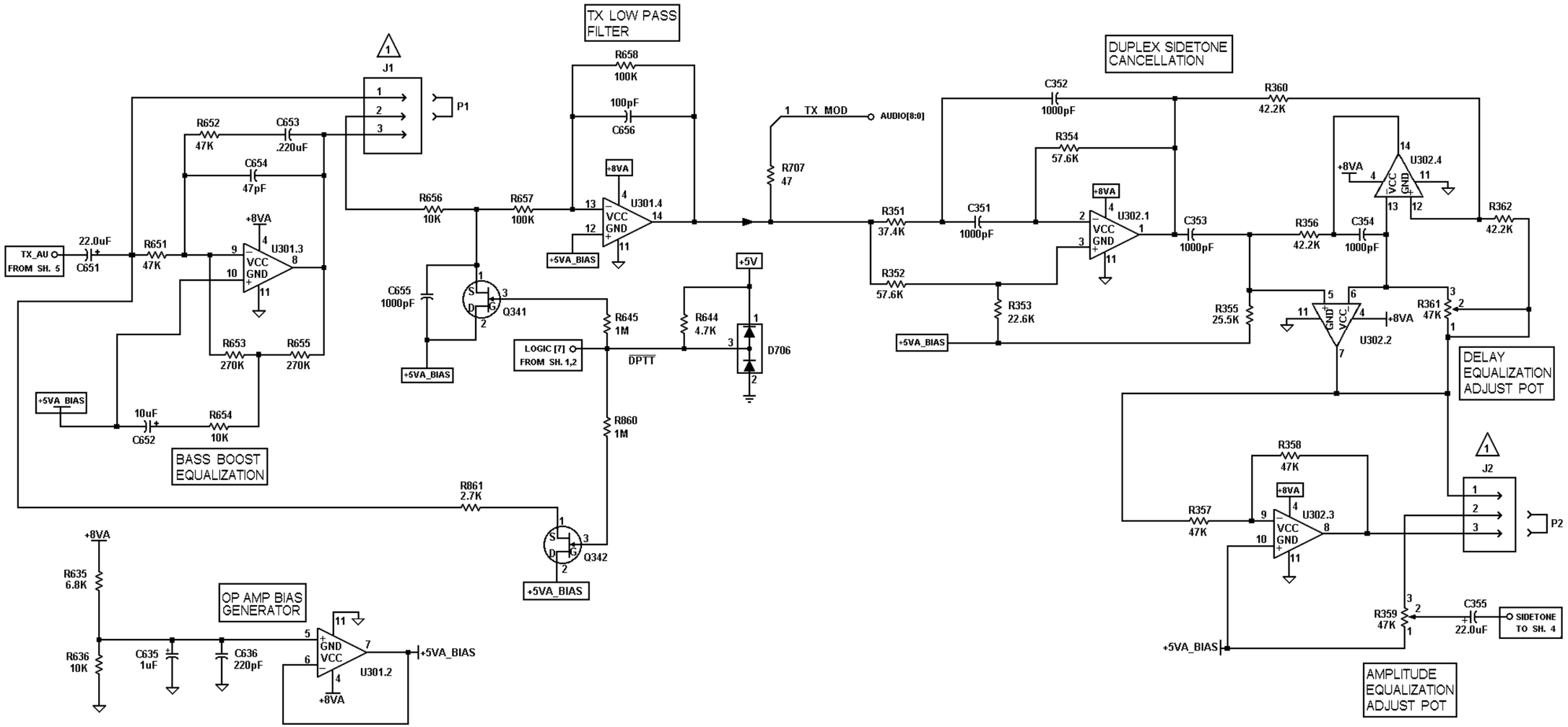
(19D904338, Sh. 4, Rev. 9)



TX AUDIO PORTION OF U804, AUDIO SIGNAL PROCESSOR
BLOCK DIAG SHOWN FOR REF ONLY

AUDIO/LOGIC BOARD
19D903963G1
Sheet 5 of 6

(19D904338, Sh. 5, Rev. 9)



AUDIO/LOGIC BOARD
19D903963G1
Sheet 6 of 6

(19D904338, Sh. 6, Rev. 9)